barcode pattern for information management on a lead frame to which semiconductor chips are bonded.

21. (Amended) A semiconductor device according to claim 1, wherein said two-dimensional code pattern is formed on said semiconductor chip by photolithography.

REMARKS

The Office Action of February 7, 2002, and the references cited therein have been carefully considered.

In this Amendment the application has been amended to delete the phrase "matrix code" as required by the Examiner. No other change in the scope of the claims has been made.

The objection to the Amendment filed October 18, 2001 and the rejection of all of the claims, i.e., claims 1-21, under 35 U.S.C. § 112, first paragraph, for the reason that there is no support for the term "matrix code" in the original application papers has been noted. In response thereto, the term "matrix code" has been deleted from the application. Accordingly, the objection to the Amendment and the rejection of the claims under 35 U.S.C. § 112, first paragraph are no longer warranted and should be withdrawn.

Reconsideration of the rejection of claims 1-21 under 35 U.S.C. § 103(a) as being unpatentable over the patent to Merlin et al. in view of the patents to Shamir and Wang et al. is respectfully requested. The primary reference to Merlin, et al. (which corresponds to U.S. Patent No. 5,552,574) and the Shamir reference and the differences between same and the present invention have been extensively discussed in the prior Amendments. Accordingly, the

comments presented therein are incorporated herein by reference rather than repeating same. However, additional comments are made below.

The present invention is directed to the arrangement for improving the handling of semiconductor devices in various stages throughout the production thereof. According to the present invention, identifying information is disposed on the surface of a semiconductor chip, a lead frame and/or a semiconductor device, respectively, containing information about the specific semiconductor chip, the chips contained in a lead frame, and the device, respectively. One of the problems in providing such indicia, wherein the quantity of desired information can become enlarged and can increase with succeeding processing steps, is the amount of the area on the chip surface, the lead frame and/or the device which must be utilized for the indicia. Accordingly, it is necessary that the area or space used to provide the respective indicia or information not significantly reduce the size of the area available for other necessary components, for example, a circuit formed in a chip, leads of the lead frame, imprinting the semiconductor device identification and the like. According to the present invention, the information at the various stages during the manufacturing processes is provided in the form of a two-dimensional code pattern, particularly, a two-dimensional barcode pattern, comprised of a plurality of square blocks arranged in a matrix or grid in a predetermined two-dimensional region of the associated surface. Through the use of such a two-dimensional code pattern, only a very small area must be provided to accommodate the code pattern which can support an increasing volume of information that must be provided. As a result, a high degree of efficiency is achieved in the information management when manufacturing the semiconductor's devices through a number of steps. That is, the invention achieves advantages that are specifically directed to the

field of semiconductor manufacturing technology in that a two-dimensional code pattern is used in the semiconductor device production to provide the information at the desired location. It is submitted no combination of the teachings of the Merlin et al., Shamir and Wang, et al references teaches or renders obvious the novel combination of features recited in the claims.

The patent to Merlin et al. is directed to a very specific arrangement for providing information concerning a micromodule on the connective layer of the micromodule. As shown in Figure 1, the micromodule includes a semiconductor chip 16 that is mounted on one surface of a support 15 made of epoxy resin and is connected via wires 14 to respective electrical contacts 12 disposed on the opposite surface of the support 15. In order to provide some indicia, such as a trademark or a mark identifying the chip 16, the identifying indicia, in the form of letters of the alphabet is etched via a laser into the contact layers 12. Note that according to this patent, the object is to provide the indicia without in any way damaging the semiconductor device 16 itself or the conductive layers, and this is specifically achieved by etching the indicia into the contacts via a laser. No where in this patent is there any teaching or suggestion that the indicia can be placed anywhere other than on the contacts, or that it should done other than by a laser. Moreover, since the etching is to be done by a laser, it specifically teaches that the markings should not damage the chip 16, thus requiring that the laser etching and the resulting indicia not take place on the chip itself. Thus, it is clear that the Merlin et al. patent does not teach or suggest placing the indicia on a chip, on a lead frame to which semiconductor chips are bonded, or to a surface of a resin-sealant of a semiconductor device as required by the various independent claims 1, 4, 7, 11, 14, and 16. Moreover, there is no teaching or suggestion in this reference of the specific type of ID information required by at least certain of the claims, for

example, claim 4 requires that the information be frame ID information while claim 7 requires that the information be product ID information. Again, such is not the case according to the Merlin et al. patent.

In the attempt to overcome this deficiency of the Merlin et al. patent, the Examiner has cited the Shamir patent which discloses providing a label containing identifying information in the form of a conventional single dimensional bar code on the device. While this patent does recognize that it may be necessary or desirable to have more information than that which can be placed on a single microlabel, the answer to this problem according to the Shamir patent is to provide a plurality of microlabels containing the different additional information. However, there is no teaching or recognition in this patent that substantially greater amounts of data can be placed on the surface of the device in question without requiring the substantial increase in the amount of surface area required by using a two-dimensional code, particularly a bar code, as required by the claims of the present application.

It should further be noted that, contrary to the position taken by the Examiner, it is submitted that it would not be obvious to one skilled in the art to combine the teachings of the Merlin et al. and Shamir references in the manner suggested by the Examiner. That is, the Merlin et al. patent specifically teaches etching indicia into the contacts of a micromodule containing a semiconductor device. On the other hand, the Shamir patent specifically teaches fixing a label with a bar code to a device or portions thereof during the manufacturing process. Thus, any combination of the teachings of these two references would result either in applying bar codes to the contacts in the Shamir arrangement by etching, which would not constitute Applicant's claimed invention, or possibly using the laser of Merlin et al. to etch bar codes into

the devices of Shamir, which would not be considered by one skilled in the art as it would damage the devices in question. Accordingly, it is submitted that no combination of the teachings of these two references would result in the invention defined in any of claims 1-21.

It should additionally be noted that while the Wang et al patent does teach the inter-changeability of two-dimensional matrix codes and two-dimensional bar codes, it teachings same in the general context of data transmission or data representation. However, it does not teach that such a two-dimensional bar code would have any special applicability in the semiconductor manufacturing arena or that it should be used to conserve surface area. Since neither the Merlin et al. nor the Shamir reference recognizes the problem to be solved according to the present invention in the semiconductor manufacturing field and the specific manner in which this problem is solved, and since the Wang et al patent is from a different technological field and thus is non-analogous art, it is submitted that one skilled in the art having the cited reference before him would not consider combining these three references in the manner suggested by the Examiner, except through the use of hindsight in the light of Applicant's invention.

Finally, it should be noted that independent claims 11, 14, and 16, and consequently the claims dependent thereon are all directed to information management systems which require a read device that reads a specific type of information provided on a chip, a lead frame, or a device in a two-dimensional code pattern comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region, and a management unit that reads the chip information and manages individual semiconductor manufacturing processes. None of the cited references discloses any such device for specific types of information including a read device and a management unit that responds to the output of the read device and manages individual

semiconductor manufacturing processes based upon the read information. It is noted that the Examiner has not commented on the limitations of these claims, nor pointed out where they are found in the references in any of the prior art rejections. Accordingly, for these additional reasons, it is submitted that claims 11-20 are allowable over the cited combination of references.

In view of the above amendments, and for the above stated reasons, it is submitted that all of the pending claims are allowable over the prior art of record and are in condition for allowance. Such action and the passing of this application to issue therefor are respectfully requested.

If the Examiner is of the opinion that the prosecution of this application would be advanced by a personal interview, the Examiner is invited to telephone the undersigned counsel to arrange for such an interview.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The following paragraphs in the originally-filed specification have been amended as follows:

The paragraphs on page 5, beginning at line 12 to page 6, line 10 have been amended as follows:

In order to achieve the objects stated above, in a first aspect of the present invention, a semiconductor device is provided that is characterized in that a two-dimensional barcode [or matrix code] pattern for information management is projected and exposed as chip ID information on each of the chips arrayed on the wafer surface. It is to be noted that since chip ID information is provided in the two-dimensional barcode pattern, it becomes possible to make use of chip information that is inherent to each chip.

Since the quantity of information that can be recorded per unit area of a two-dimensional code pattern is very large and recognition utilizing an optical apparatus can be implemented with ease, marking can be made on each of the chips arrayed on the wafer surface, which has not been possible in the prior art, so the information management can be easily implemented for chips on an individual basis.

In addition, as a method for marking a two-dimensional barcode pattern on each chip, projection and exposure may be implemented by employing a liquid crystal mask capable of changing transmitted patterns for different exposures to provide different chip ID information for each wafer using the same mask.

In order to achieve the objects described above, in a second aspect of the present invention, a semiconductor device is provided that is characterized in that marking is implemented with two-dimensional code patterns for information management as framed ID information on lead frames to which semiconductor chips are bonded. It is to be noted that in the frame ID information in the two-dimensional code pattern, chip positional information indicating the position of chips within the frame and the chip ID information may be included.

The paragraph on page 8 spanning lines 20-22 has been amended as follows:

FIG. 1 illustrates a schematic structure of an embodiment of a two-dimensional [matrix] code pattern that may be adopted in the present invention;

The paragraph on page 8 spanning lines 25-27 has been amended as follows:

FIG. 3 [illustrated] illustrates an embodiment of a two-dimensional [matrix] code pattern [forward] formed on a semiconductor chip according to the present invention;

The paragraph on page 8 spanning lines 28-31 has been amended as follows:

FIG. 4 [illustrated] illustrates an embodiment of the liquid crystal mask employed to project and expose a two-dimensional [matrix] code pattern on a semiconductor chip according to the present invention;

The paragraph on page 9 spanning lines 16-20 has been amended as follows:

FIG. 10 is a block diagram illustrating the schematic structure of a die bonder that is capable of adding a two-dimensional[; matrix] code pattern to a lead time during the bonding step according to the present invention;

The paragraph on page 10 spanning lines 7-9 has been amended as follows:

FIG. 17 illustrates a state in which character information and a two-dimensional [matrix] code pattern are printed at the package;

The paragraph on page 10 spanning line 33 to page 11, line 17 has been amended as follows:

First, in FIG. 1, an example of a two-dimensional code pattern and in particular a two-dimensional barcode [or matrix code] pattern which may be employed in an embodiment of the present invention is shown. As shown in the figure, a two-dimensional barcode [or matrix code] pattern 10 is a two-dimensional pattern in which specific information can be recorded by coloring the squares 11 of a grid in black or white to form blocks that extends two-dimensionally in conformance to predetermined rules. It is to be noted that while the encoding rules for coloring the grid black and white in the two-dimensional pattern may be the same as those in the prior art, new encoding rules may be created instead. A detailed explanation of the actual method for coloring the grid black and white is omitted since it does not bear direct relevance to the contents of the present invention. However, since data error detection can be encoded as part of the encoding rules, and in that case, errors when reading two-dimensional barcode patterns

recorded at individual chips, individual frames and individual resin-sealed semiconductor chips can be reduced, as detailed later.

The paragraph on page 12 spanning line 4-9 has been amended as follows:

In contrast, the inventor of the present invention has observed that the two-dimensional barcode [or matrix code] pattern adopted in the present invention provides the following superior features compared to the character information patterns and one-dimensional barcode patterns in the prior art.

The paragraphs on page 12 spanning line 29 to page 13 line 5 have been amended as follows:

The inventor of the present invention has conducted focused research into the features of the two-dimensional code patterns described above, which has cumulated in the completion of the present invention, which achieves efficient and accurate information management in the inter-process physical distribution in the semiconductor manufacturing processes by utilizing two-dimensional code patterns at various stages in the semiconductor manufacturing processes.

The following is a detailed explanation of embodiments in which two-dimensional [barcode i.e. matrix] codes e.g., barcodes, according to the invention are used at various stages in the semiconductor manufacturing processes.

IN THE CLAIMS:

Claims 1, 4, 6, 7, 9, 10 14, 16, 17,18 and 21 are amended as follows:

1. (Five Times Amended) A semiconductor device having at least one semiconductor chip manufactured from a wafer, said semiconductor chip comprising said device and having a two-dimensional [matrix] code pattern for information management provided on a surface of said at least one semiconductor chip with the pattern representing chip ID information, and said two-dimensional [matrix] code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

4. (Four Times Amended) A semiconductor device manufactured using a lead frame, with the lead frame having a two-dimensional [matrix] code pattern for information management provided on said lead frame to which semiconductor ships are bonded, with the pattern representing frame ID information, and said two-dimensional [matrix] code pattern is comprised of a plurality of square blocks arranged in a grid in a predetermined two-dimensional region.

6. (Twice Amended) A semiconductor device according to claim 4, wherein: said frame ID information is made to correspond to chip ID information provided as a two-dimensional [matrix] barcode pattern for information management for each chip.

7. (Four Times Amended) A semiconductor device having at least one semiconductor chip sealed by resin, and having a two-dimensional [matrix] code pattern for information management provided at an outer surface of said resin and representing product ID

information, and said two-dimensional [matrix] code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

9. (Twice Amended) A semiconductor device according to claim 7, wherein: said product ID information corresponds to chip ID information provided as a two-dimensional [matrix] barcode pattern for information management for each chip.

10. (Twice Amended) A semiconductor device according to claim 7, wherein: said product ID information corresponds to frame ID information provided as a two-dimensional [matrix] barcode pattern for information management on a lead frame to which semiconductor chips are bonded.

11. (Four Times Amended) An information management system for semiconductor devices, having at least one semiconductor chip that implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads chip ID information, said chip ID information is provided on said semiconductor chip as a two-dimensional [matrix] barcode pattern for information management for each chip, said two-dimensional [matrix] barcode pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

information, and said two-dimensional [matrix] code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

9. (Twice Amended) A semiconductor device according to claim 7, wherein: said product ID information corresponds to chip ID information provided as a two-dimensional [matrix] barcode pattern for information management for each chip.

10. (Twice Amended) A semiconductor device according to claim 7, wherein: said product ID information corresponds to frame ID information provided as a two-dimensional [matrix] barcode pattern for information management on a lead frame to which semiconductor chips are bonded.

11. (Four Times Amended) An information management system for semiconductor devices, having at least one semiconductor chip that implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads chip ID information, said chip ID information is provided on said semiconductor chip as a two-dimensional [matrix] barcode pattern for information management for each chip, said two-dimensional [matrix] barcode pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said chip ID information thus read and manages individual semiconductor manufacturing processes based upon said chip ID information thus registered.

14. (Four Times Amended) An information management system for semiconductor device manufactured using a lead frame, which system implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads frame ID information, said frame ID information is provided on said lead frame as a two-dimensional [matrix] code pattern for information management, said two-dimensional [matrix] code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said frame ID information thus read and manages individual semiconductor manufacturing processes based upon said frame ID information thus registered.

16. (Four Times Amended) An information management system for semiconductor devices having semiconductor chips sealed by resin, which system implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads product ID information, said product ID information is provided as a two-dimensional [matrix] code pattern for information management at an outer surface of

said resin, said two-dimensional [matrix] code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said product ID information thus read and manages a product shipping process based upon said product ID information thus registered.

17. (Twice Amended) An information management system for semiconductor devices according to claim 16, wherein: said product ID information corresponds to chip ID information provided as a two-dimensional [matrix] barcode pattern for information management for each chip.

18. (Twice Amended) A semiconductor device according to claim 16, wherein: said product ID information corresponds to frame ID information provided as a two-dimensional [matrix] barcode pattern for information management on a lead frame to which semiconductor chips are bonded.

21. (Amended) A semiconductor device according to claim 1, wherein said two-dimensional [matrix] code pattern is formed on said semiconductor chip by photolithography.